

CLAIMS

What is claimed is:

1. A semiconductor memory comprising:
an array including a redundant row;
a first set of non-volatile elements for storing at least a portion of an address of a defective cell of said array;
data path circuitry coupled to said array for writing data thereto and reading data therefrom;
a second set of non-volatile elements for storing a block repair configuration;
routing circuitry coupled to said second set of non-volatile elements capable of being configured by a stored block repair configuration to output a selected ratio of received row address bits to received column address bits; and
comparison circuitry coupled to said first set of non-volatile elements, said data path circuitry, and said routing circuitry for comparing row and column address bits output by said routing circuitry with said stored at least a portion of said defective cell address and, when a match occurs, for implementing a block repair of said defective cell by activating said redundant row and directing said data path circuitry to write data to or read data from said activated redundant row.

2. The semiconductor memory of claim 1, wherein said array is a magnetic random access memory (MRAM) array, dynamic RAM (DRAM) array, synchronous DRAM (SDRAM) array, double data rate SDRAM (DDR SDRAM) array, RAMBUS® DRAM (RDRAM®) array, extended data-out DRAM (EDO DRAM) array, fast-page-mode DRAM (FPM DRAM) array, static random access memory (SRAM) array, SyncBurst™ SRAM array, Zero Bus Turnaround™ SRAM (ZBT™ SRAM) array, Quad Data Rate™ SRAM (QDR™ SRAM) array, DDR synchronous SRAM (DDR SRAM) array or nonvolatile electrically block-erasable programmable read only memory (Flash) array.

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3. The semiconductor memory of claim 1, wherein said first and second sets of non-volatile elements including at least one of fuses, anti-fuses, and flash EEPROM cells.

4. The semiconductor memory of claim 1, wherein said first set of non-volatile elements comprises non-volatile elements for storing at least a portion of a row address and at least a portion of a column address of said defective cell.

5. The semiconductor memory of claim 1, wherein said routing circuitry comprises select circuitry and multiplexer (mux) circuitry.

6. The semiconductor memory of claim 5, wherein said select circuitry comprises inverters, NOR gates, and NAND gates, and wherein said mux circuitry comprises multiplexers and inverters.

7. The semiconductor memory of claim 1, wherein said second set of non-volatile elements includes a block repair enabling non-volatile element for enabling block repairs when active and disabling block repairs, and thereby enabling conventional row repairs, when inactive.

8. The semiconductor memory of claim 7, wherein said first set of non-volatile elements stores only row address bits of said defective cell.

9. The semiconductor memory of claim 1, wherein said comparison circuitry comprises circuitry for implementing a block repair that does not cross logical boundaries within said array.

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10. A Static Random Access Memory (SRAM) comprising:
a SRAM array including a redundant row;
bad address storage fuses for storing at least a portion of an address of a defective cell of said
SRAM array;
data path circuitry coupled to said SRAM array for writing data thereto and reading data
therefrom;
row and column decoders coupled to said SRAM array for selecting cells therein in accordance
with received row and column addresses;
selection fuses for storing a block repair configuration;
selection and multiplexer (mux) circuitry coupled to said selection fuses capable of being
configured by a stored block repair configuration to output a selected ratio of received
row address bits to received column address bits; and
comparison circuitry coupled to said bad address storage fuses, said data path circuitry, said
SRAM array column decoder, and said selection and mux circuitry for comparing row
and column address bits output by said selection and mux circuitry with said stored at
least a portion of said defective cell address and, when a match occurs, for implementing
a block repair of said defective cell by activating said redundant row and by directing said
data path circuitry to write data to or read data from said activated redundant row.

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11. A block repair device for a semiconductor memory having an array including a redundant row, said block repair device comprising:
a set of non-volatile elements for storing a block repair configuration;
routing circuitry coupled to said set of non-volatile elements capable of being configured by a stored block repair configuration to output a selected ratio of received row address bits to received column address bits; and
comparison circuitry coupled to said routing circuitry for comparing row and column address bits output by said routing circuitry with a stored portion of an address of a defective cell of said array and, when a match occurs, for implementing a block repair of said defective cell by activating said redundant row and causing data to be written to or read from said activated redundant row of said array.

12. A semiconductor substrate on which is fabricated a semiconductor memory comprising:
an array including a redundant row;
a first set of non-volatile elements for storing at least a portion of an address of a defective cell of said array;
data path circuitry coupled to said array for writing data thereto and reading data therefrom;
a second set of non-volatile elements for storing a block repair configuration;
routing circuitry coupled to said second set of non-volatile elements capable of being configured by a stored block repair configuration to output a selected ratio of received row address bits to received column address bits; and
comparison circuitry coupled to said first set of non-volatile elements, said data path circuitry, and said routing circuitry for comparing row and column address bits output by said routing circuitry with said stored at least a portion of the defective cell address and, when a match occurs, for implementing a block repair of the defective cell by activating said redundant row and directing said data path circuitry to write data to or read data from said activated redundant row within said array.

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13. The semiconductor substrate of claim 12 wherein the substrate comprises a semiconductor wafer.

14. An electronic system comprising an input device, an output device, a memory device, and a processor device coupled to said input device, said output device, and said memory device, at least one of said input device, said output device, said memory device, and said processor device including a semiconductor memory, comprising:

- an array including a redundant row;
- a first set of non-volatile elements for storing at least a portion of an address of a defective cell of said array;
- data path circuitry coupled to said array for writing data thereto and reading data therefrom;
- a second set of non-volatile elements for storing a block repair configuration;
- routing circuitry coupled to said second set of non-volatile elements capable of being configured by a stored block repair configuration to output a selected ratio of received row address bits to received column address bits; and
- comparison circuitry coupled to said first set of non-volatile elements, data path circuitry, and said routing circuitry for comparing row and column address bits output by said routing circuitry with said stored at least a portion of said defective cell address and, when a match occurs, for implementing a block repair of said defective cell by activating said redundant row and directing said data path circuitry to write data to or read data from said activated redundant row of said array.

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15. A block repair method for a semiconductor memory having an array including a defective cell and a redundant row, said block repair method comprising:
selecting dimensions of a repair block within said array for repairing said defective cell;
programming non-volatile elements within said semiconductor memory to store row and column address bits of said defective cell defining said selected dimensions of said repair block;
programming other non-volatile elements within said semiconductor memory to store a block repair configuration corresponding to said selected dimensions of said repair block;
in accordance with said stored block repair configuration, routing received row and column address bits to determine whether a received address falls within said repair block for comparison with said stored row and column address bits of said defective cell; and
when a match occurs, firing said redundant row and writing data to or reading data from a cell within said redundant row selected in accordance with said row and column address bits of said defective cell not stored by said non-volatile elements.

16. The block repair method of claim 15, wherein said programming non-volatile elements comprise programming non-volatile elements comprising at least one of fuses, anti-fuses, and flash EEPROM cells.

17. The block repair method of claim 15, wherein said programming other non-volatile elements comprise programming other non-volatile elements comprising at least one of fuses, anti-fuses, and flash EEPROM cells.

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18. A block repair method for a semiconductor memory having an array including a defective cell and a redundant row, said block repair method comprising:
selecting dimensions of a repair block within said array for repairing said defective cell;
storing row and column address bits of said defective cell defining said selected dimensions of said repair block;
storing a block repair configuration corresponding to said selected dimensions of said repair block;
in accordance with said stored block repair configuration, routing received row and column address bits to determine whether a received address falls within said repair block for comparison with said stored row and column address bits of said defective cell; and
when a match occurs, firing said redundant row and writing data to or reading data from a cell within said redundant row selected in accordance with any non-stored row and column address bits of said defective cell.

19. The block repair method of claim 18, wherein said storing row and column address bits and said storing a block repair configuration comprise programming non-volatile elements comprising at least one of fuses, anti-fuses, and flash EEPROM cells.

20. The block repair method of claim 18, wherein said routing received row and column address bits comprises multiplexing received row and column address bits in accordance with said block repair configuration.

21. The block repair method of claim 18, wherein said storing a block repair configuration includes programming a non-volatile element to enable block repair with respect to said redundant row.

22. The block repair method of claim 18, wherein said storing a block repair configuration includes programming a non-volatile element to disable block repair with respect to said redundant row and thereby enable conventional row repair using said redundant row.

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23. The block repair method of claim 18, wherein said storing row and column address bits of said defective cell defining said selected dimensions of said repair block comprises storing only row address bits of said defective cell.

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